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ANALYSIS OF VARIOUS TOPOLOGIES OF FDCCII AND ITS APPLICATIONS

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ABSTRACT

In this paper, various topologies of fully differential second-generation current conveyor (FDCCII) are presented. The proposed blocks are useful in mixed-mode applications where fully differential signal processing is required. The FDCCII combines the advantages of both second-generation current conveyor (CCII) and differential difference amplifier (DDA), which is further utilized to realize Universal Biquad filters. The circuit can operate from low supply voltages down to 1.65 V. The characteristics of the proposed circuits are verified by LTSPICE simulators using TSMC CMOS 0.35-µm technology.

KEYWORDS: Fully Differential Second Generation current conveyor, Differential Difference Amplifier, Universal Biquad Filter.

I. INTRODUCTION

An analog circuit design using the current mode approach has recently gained considerable attention. This stems from its inherent advantages such as wide bandwidth, high slew rate, low power consumption, and simple circuitry [1]. The second generation current conveyor (CCII) is one of the most versatile current mode building blocks. Since its introduction [2], it has been used in a wide range of applications, and several circuit realizations have been proposed for its implementation [3]-[8]. The CCII is a single-ended device; however, most modern high-performance analog integrated circuits incorporate fully differential signal paths. This is because fully-differential circuit configurations have been widely used in high-frequency analog signal applications such as switched capacitor filters [9] and mute-standard wireless receivers [10]. As compared to their single-ended counterparts, they have higher rejection capabilities to clock-feed-through, and to charge injection errors and power supply noises. They also have a larger output dynamic range, higher design flexibility, and reduced harmonic distortion. Moreover, most modern systems employ both analog and digital parts on the same chip. Fully-differential architecture of the analog part becomes more essential as it provides immunity to digital noise.

In this paper, various topologies of fully-differential CMOS second generation current conveyor (FDCCII) are proposed. The FDCCII has been designed to improve the dynamic range and to suppress all undesirable common-mode signals. This active element has plus/minus y-terminals, plus/minus x-terminals and plus/minus z-terminals; hence with a single device the arithmetic operation capability of voltage signals and addition/subtraction of current signals can be easily obtained. The FDCC can also be considered as a differential version of the current conveyor. The FDCCII has the advantages of the single-ended CCII along with the advantages of fully-differential signal processing.

II. FULLY DIFFERENTIAL CURRENT CONVEYOR (FDCCII)

The FDCCII is basically a fully differential device as shown in Figure.1. The Y1 and Y2 terminals are high impedance terminals while X1 and X2 terminals are low impedance ones.

The differential input voltage VY12 applied across Y1 and Y2 terminals is conveyed to differential voltage across the X1 and X2 terminals; i.e., (VX12 =VY12). The input currents applied to the X1 and X2 are conveyed to the Z1 and Z2 terminals that is, (Iz1=Ix1 and Iz2=Ix2). The Z1 and Z2 terminals are high impedance nodes suitable for current outputs.

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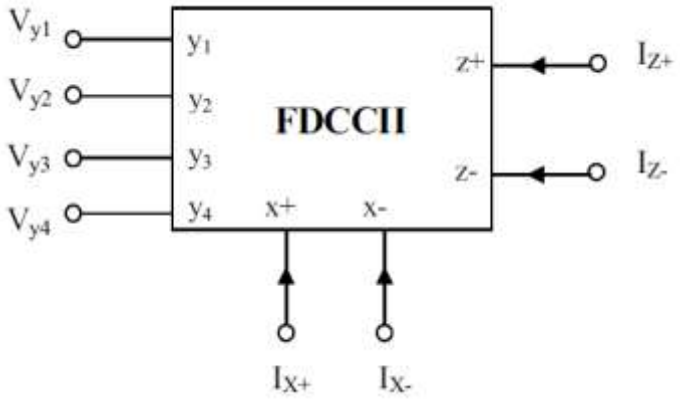

Figure 1: The circuit symbol of the FDCCII [11]

Considering the non-idealities arising from the physical implementation of the FDCCII, its terminal relationship can be characterized by:

$$\begin{bmatrix} V_{X+} \\ V_{X-} \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \beta_1 & -\beta_2 & \beta_3 & 0 \\ 0 & 0 & -\beta_1 & \beta_2 & 0 & \beta_4 \\ \alpha_p & 0 & 0 & 0 & 0 & 0 \\ 0 & \alpha_N & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{X+} \\ I_{X-} \\ V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ V_{Y4} \end{bmatrix}$$

where ideally β1=β2=β3=β4=1 and αN=αP=1 that represent the voltage and current transfer ratios of the FDCCII respectively. By applying nodal analysis and referring to above matrix, the characteristic equation of the circuit can be expressed as

$$V_O = \frac{s^2 R_1 R_2 R_3 C_1 C_2 V_{in3} - sR_2 R_3 C_2 V_{in2} + R_3 V_{in1}}{s^2 R_1 R_2 R_3 C_1 C_2 + sR_1 R_2 C_2 + R_3} \qquad (1)$$

III. VARIOUS TOPOLOGIES OF FDCCII

FDCCII implementation can be done by using NMOS and PMOS transistors in various combinations. Here, we have represented three different circuit configurations that consist of varying number of transistors. Topology 1 of the CMOS implementation of FDCCII is shown in Figure.2. It consists of total sixty numbers of MOSFETs, along with few voltage and current source. All transistors are assumed to be operating at saturation. The aspect ratios for the transistors are mentioned below, which can be kept similar for all NMOS and PMOS or may be kept different from each other depending upon the requirement of the operation that is to be performed by the device.

Similarly Figure.3 and Figure.4 shows the Topology 2 and Topology 3 of the FDCCII CMOS implementation, in which topology 2 consists of about thirty-six transistors whereas topology 3 comprises forty-four transistors. The main idea behind varying the number of transistor usage is to reduce the area occupied by the device, which itself would result in reducing the power consumption of the whole circuit resulting in improved circuit performance along with less power dissipation, which nowadays have become the main point of concern for the devices being utilized in the electronics industry or even for the basic electronic components being utilized for daily household purposes.

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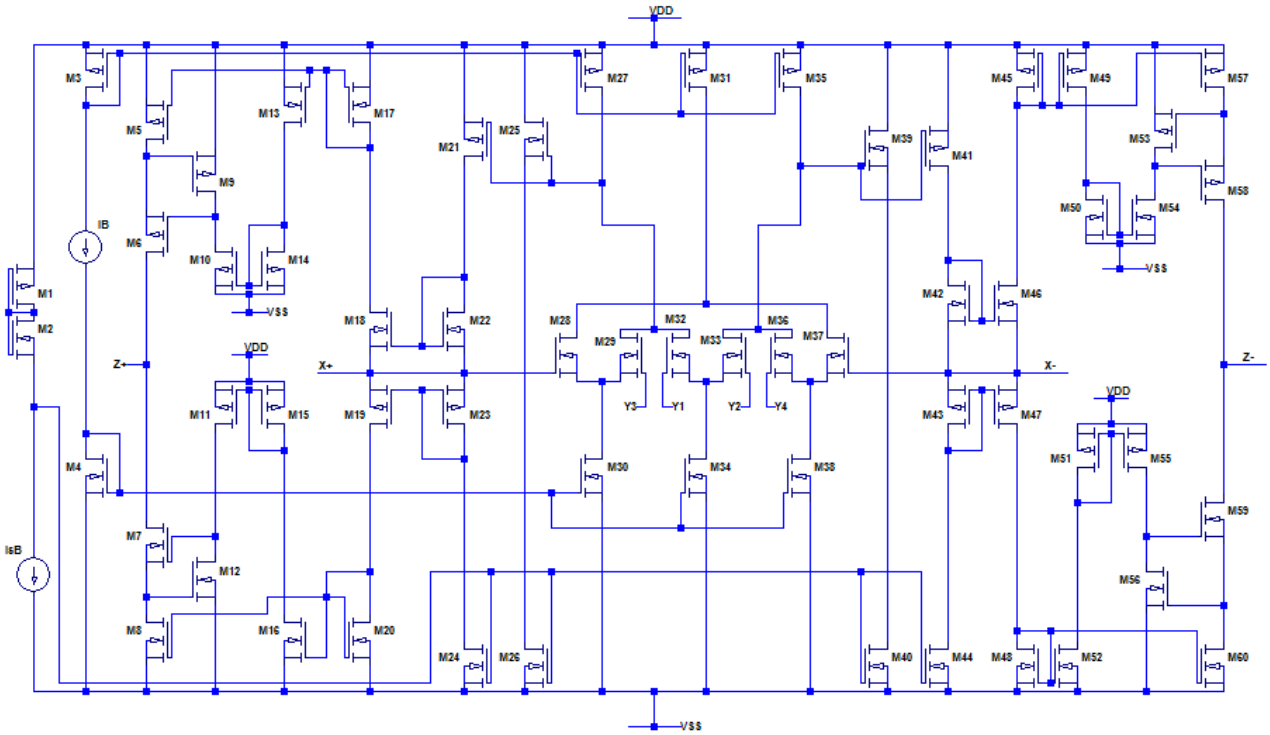

Figure 2: Topology 1 CMOS implementation of FDCCII [13]

FDCCII finds various applications in the field of analog computation, Current conveyors can be used through various methods, example current summer, weighted current summer, current amplifier, current differentiator and current integrator. They are basically used as effective building blocks in order to realize countless current mode active filters. A universal filter is most famous analog filter as it can be able to determine standard functions like low pass, high pass, band reject, band pass and all pass. They are also helpful in the active network synthesis and can be used in number of configurations, i.e. voltage controlled voltage source, current controlled voltage source, voltage controlled current source, current controlled current source, gyrator etc. Filters and oscillators designing can be done very effectively with the help of current conveyor. [12]

FDCCII combines the advantages of both second-generation current conveyor (CCII) (such as wide bandwidth, high linearity and wide dynamic range) and differential difference amplifier (DDA) (such as high-input impedance and versatile addition and subtraction voltage capability) into a single device. Thus, addition and subtraction signals for voltage-mode operation can be obtained easily using FDCCII. Moreover, most modern systems employ both analog and digital parts on the same chip. Fully-differential architecture of the analog part becomes more essential as it provides immunity to digital noise.

The supply voltages were given as $V_{DD} = -V_{SS} = 1.65$ V. The bias voltages were chosen as $V_{bp} = -V_{bn} = 0$ V and the bias currents were chosen as $I_B = I_{SB} = 125$ µA

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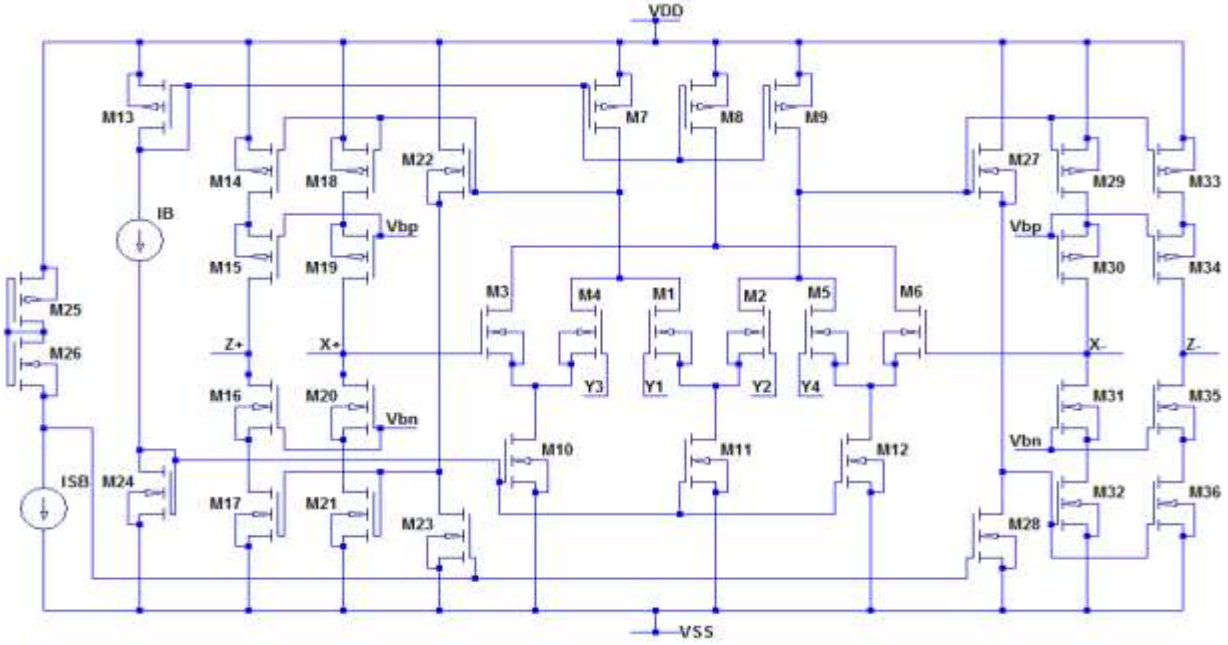

Figure 3: Topology 2 CMOS implementation of FDCCII [13]

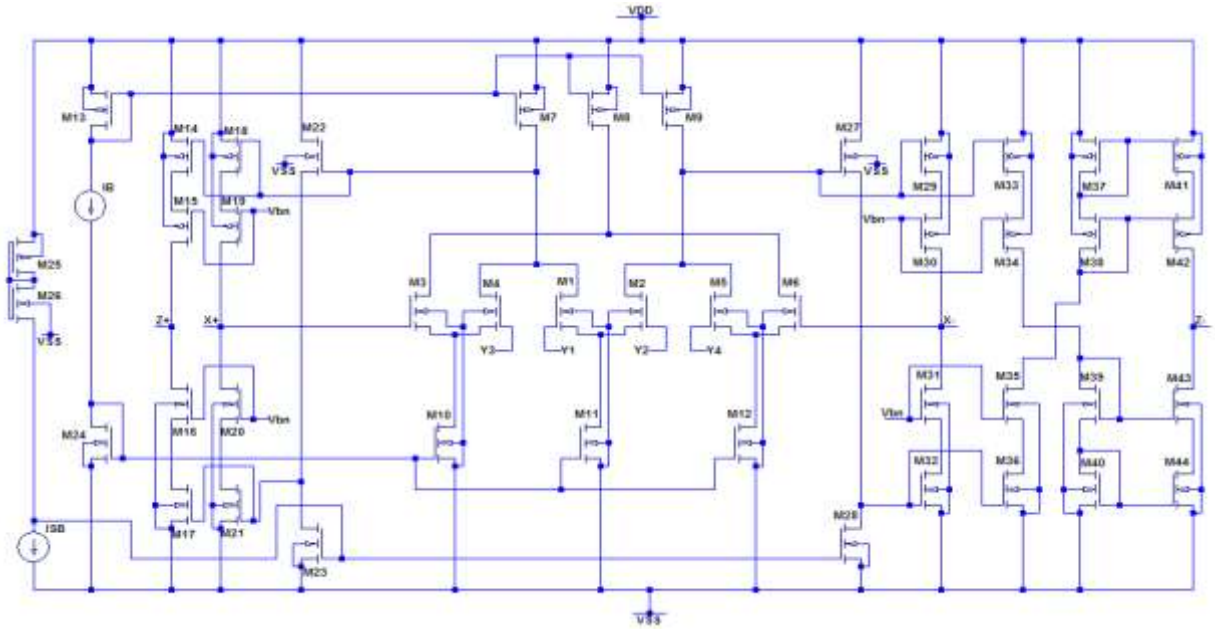

Figure 4: Topology 3 CMOS implementation of FDCCII [14]

The aspect ratios of the MOS transistors for the Topology 1 and 2 circuits are given in Tables 1 and 2 respectively. However the transistor aspect ratios for the Topology 3 circuit were given as 5µm/1µm for all NMOS transistors and 10µm/1µm for all PMOS transistors. The performance of the all the above topologies can be verified and compared using the LTSPICE simulation program. The MOS transistors are simulated using Taiwan semiconductor manufacturing company (TSMC) CMOS 0.35-µm process model parameters. Note that the proposed FDCCII structure is also realizable with other sub-micron CMOS technologies using adequate transistor dimensions without changing the analogue circuit topology and performance.

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Table 1: Transistors aspect ratios for the Topology 1 circuit

Transistors	W (µm)	L (µm)
M_7, M_8, M_{10}, M_{12}, M_{14}, M_{16}, M_{20}, M_{28}, M_{29}, M_{32}, M_{33}, M_{36}, M_{37}, M_{48}, M_{50}, M_{52}, M_{54}, M_{56}, M_{59}, M_{60}	8.75	0.7
M_3, M_{27}, M_{31}, M_{35}	70	0.7
M_4, M_{30}, M_{34}, M_{38}	17.5	0.7
M_{25}, M_{26}, M_{39}, M_{40}	0.7	0.7
M_1, M_5, M_6, M_9, M_{11}, M_{13}, M_{15}, M_{17}, M_{21}, M_{41}, M_{45}, M_{49}, M_{51}, M_{53}, M_{55}, M_{57}, M_{58}	35	0.35
M_2, M_{18}, M_{22}, M_{24}, M_{42}, M_{44}, M_{46}	8.75	0.35
M_{19}, M_{23}, M_{43}, M_{47}	105	0.7

Table 2: Transistors aspect ratios for the Topology 2 circuit

Transistors	W (µm)	L (µm)
$M_1 – M_6$	8.75	0.7
$M_7 – M_9$, M_{13}	70	0.7
$M_{10} – M_{12}$, M_{24}	17.5	0.7
M_{14}, M_{15}, M_{18}, M_{19}, M_{25}, M_{29}, M_{30}, M_{33}, M_{34}	35	0.35
M_{16}, M_{17}, M_{20}, M_{21}, M_{26}, M_{31}, M_{32}, M_{35}, M_{36}	8.75	0.35
M_{22}, M_{23}, M_{27}, M_{28}	0.7	0.7

IV. APPLICATION EXAMPLE AND SIMULATION RESULT

The application example of multifunction filter is shown in Figure.5. The circuit is composed of only one FDCCII, two capacitors and three resistors. It should be noted that the structure offers low complexity by using only single active device. The FDCCII circuit can be constructed by making use of any of the above topologies.

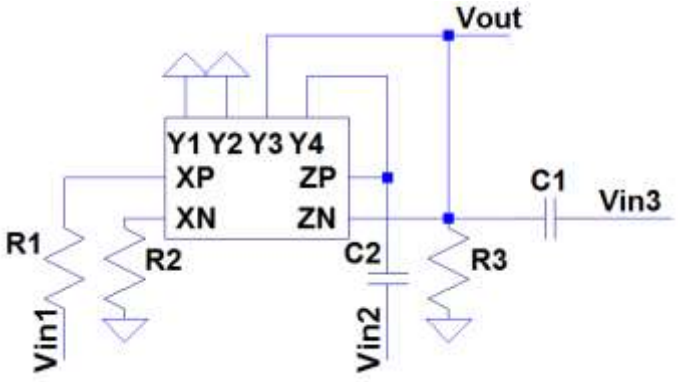

Figure 5: Application example of voltage-mode multifunction filter using FDCCII [14]

The filtering functions can be obtained by following conditions:

(i) LP: $V_{in2} = V_{in3} = 0$ (grounded) and $V_{in1} = V_{in}$;
(ii) BP: $V_{in1} = V_{in3} = 0$ (grounded) and $V_{in2} = V_{in}$;
(iii) HP: $V_{in1} = V_{in2} = 0$ (grounded) and $V_{in3} = V_{in}$;
(iv) BS: $V_{in1} = V_{in3} = V_{in}$ and $V_{in2} = 0$ (grounded);
(v) AP: $V_{in1} = V_{in2} = V_{in3} = V_{in}$ and $R_1 = R_3$.

Therefore, the proposed filter provides five standard filtering functions without inverting-type input signal as well as double input single and changing circuit topology. However, for realizing AP filter, the circuit needs passive component matching condition. A new three-input one-output voltage-mode multifunction filter has been designed using one fully differential current conveyor as an active element, and two capacitors, three resistors as passive components [15]. Universal biquadratic filter is the basic building block that typically provides several filtering functions into one single structure such as low-pass (LP), high-pass (HP), band-pass (BP) and band-stop (BS) filtering functions. The biquadratic filters are the second-order filters that can be used to realize high-order filters, and they can also be used in communication and control systems.

The parameters $C_1=C_2=10$ pF and $R_1=R_2=R_3=$ 15.9 kΩ was designed to obtain the LP, BP, HP, BS and AP

responses with $f_o \cong 1$ MHz and Q = 1. The simulated frequency responses of LP, BP, HP and BS filters were shown in Figures.6-9. Figure.10 shows the simulated frequency responses of the magnitude and phase characteristics of the AP filter. Therefore, the simulation results in Figures.6-10 can be confirmed that the filter in Figure.5 provides five standard filter responses into one single topology.

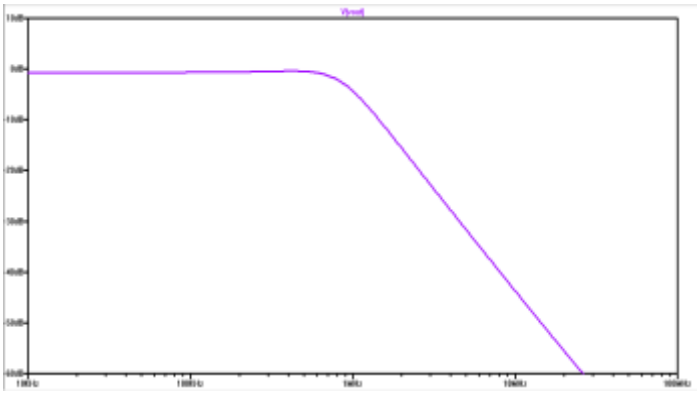

Figure 6: Low-pass filter voltage response

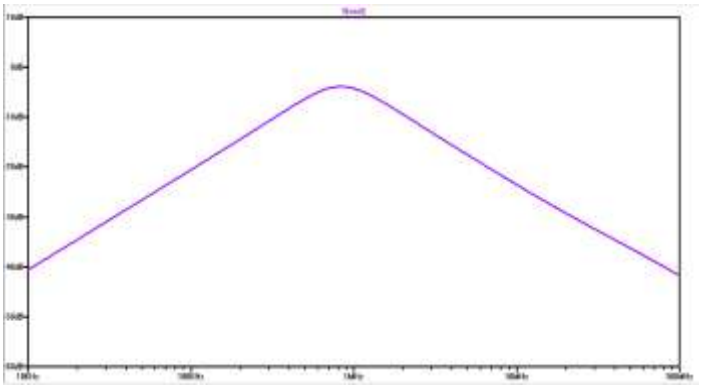

Figure 7: Band-pass filter voltage response

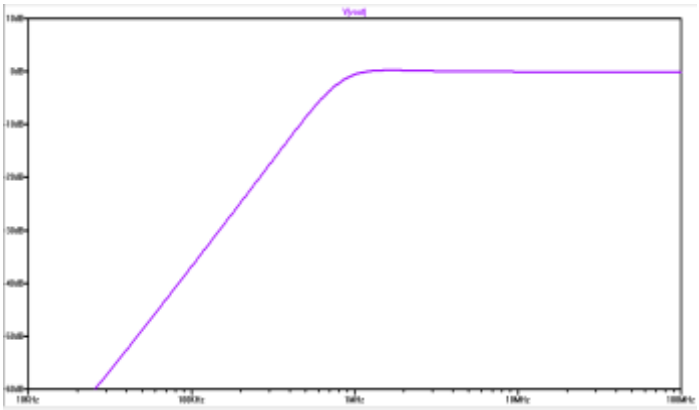

Figure 8: High-pass filter voltage response

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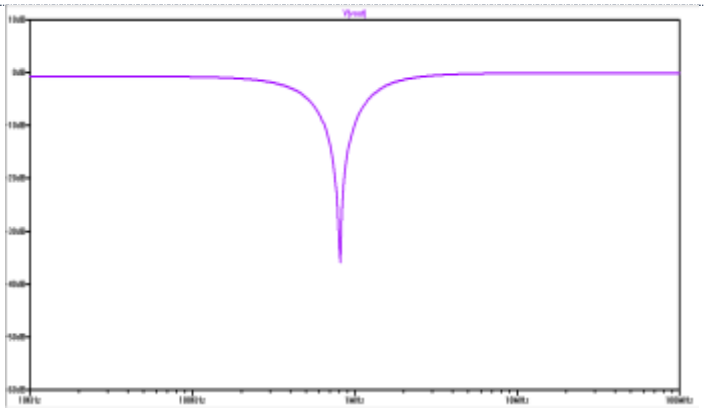

Figure 9: Band-stop filter voltage response

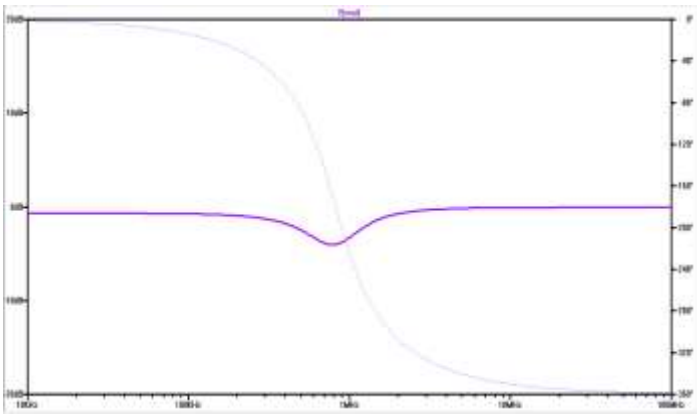

Figure 10: Simulated gain and phase responses of the AP filter

V. CONCLUSION

In this paper, various topologies of CMOS implementation of FDCCII have been presented. The proposed blocks are useful in mixed-mode applications where fully differential signal processing is required. The FDCCII combines the advantages of both second-generation current conveyor (CCII) and differential difference amplifier (DDA), which is further utilized to realize Universal Biquad filters. A new three-input one-output voltage-mode multifunction biquadratic filter using one FDCCII, two capacitors and three resistors is realized to illustrate the practical use of the proposed topologies as an application example. The main advantage of this application is that the circuit uses only single active device. The proposed filter offers LP, BP, HP, BS and AP filters into one single topology without changing the configuration and requiring inverting-type input signal. We performed simulations with LTSPICE simulation program using 0.35µm TSMC CMOS technology. LTSPICE simulation results of the filter responses are in good agreement with the predicted theory. Proposed topologies will provide new possibilities for analog IC designers

VI. REFERENCES

[1] A. M. Soliman, "Novel Generation Method of Current Mode Wein Type Oscillators using Current Conveyors," Int. J. of Electronics, vol. 85, pp. 737-747, 1998.
[2] A. Sedra and K. Smith, "A Second-Generation Current Conveyor and its Applications," IEEE Trans. Circuits Syst., vol. 17, pp. 132-134, 1970.
[3] B. Wilson, "High Performance Current Conveyor Implementation, "Electron. Lett., vol. 20, pp. 990-991, 1984.
[4] M. Cheng and C. Toumazou, "3 V MOS Current Conveyor Cell for VLSI Technology," Electron. Lett., vol. 29, pp. 317-318, 1993.
[5] H. Elwan and A. Soliman, "A Novel CMOS Current Conveyor Realization with an Electronically Tunable Current-Mode Filter Suitable for VLSI," IEEE Trans. Circuits Syst. II, vol. 43, pp. 663-670, 1996,

ISSN: 2277-9655
Impact Factor: 4.116
CODEN: IJESS7

[6] S. Mahmoud and A. Soliman, "Low Voltage Rail to Rail CMOS Current Feedback Operational Amplifier and its Applications for Analog VLSI," Analog Integrated Circuits and Signal Proc., vol. 25, pp. 47-57, 2000.
[7] H. Elwan and A. Soliman, "Low Voltage Low Power CMOS Current Conveyors," IEEE Trans. Circuits Syst. I, vol. 44, pp. 828-835, 1997.
[8] S. Mahmoud and I. Awad, "Fully Differential CMOS Current Feedback Operational Amplifier," Analog Integrated Circuits and Signal Proc., vol. 43, pp. 61-69, 2005.
[9] T. Choi, R. Kaneshiro, R. Bodersen, P. Gray, W. Jett, and M. Wilcox, "High-Frequency CMOS Switched-Capacitor Filters for Communications Application," IEEE J. Solid-state Circuits, vol. 18, pp. 652-663, 1983.
[10] J. Rudell, J.-J. Ou, T. Cho, G. Chien, F. Brianti, J. Weldon, and P. Gray, "A 1.9 GHz Wide-Band IF Double Conversion CMOS Receiver for Cordless Telephone Applications," IEEE J. Solid-State Circuits, vol. 32, pp. 2071-2088, 1997.
[11] S. A. Mahmoud," New Fully Differential CMOS Second- Generation Current Conveyor" ETRI Journal, vol. 28, pp.495-501, 2006.
[12] M. Garima and M. P. Banga, "Filter realization using second generation current conveyor", Inter. Jour. of Innovative Science, Engineering & Technology (IJISET), Vol. 1 Issue 6, 2014.
[13] F. Kacar, B. Metin, H. Kuntman and O. Cicekoglu, "A new high-performance CMOS fully differential second-generation current conveyor with application example of biquad filter realisation", Inter. Jour. of Electronics, Vol. 97, pp. 499–510, 2010.
[14] M. Kumngern and P. Supavarasuwat, "A Voltage-Mode Three-Input One-Output Multifunction Filter Using Single FDCCII," 978-1-4799-6435-2/14/$31.00 ©2014 IEEE (APCC-2014).
[15] Y. Li, "A modified CDTA (MCDTA) and its applications: designing current-mode sixth-order elliptic band-pass filter," Circuits, Systems, and Signal Processing, vol. 30, pp 1383-1390, 2011

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